Amendments to the Claims

1. (CURRENTLY AMENDED) A power semiconductor device, comprising:

an output transistor ~~(2)~~ having main cells ~~(32)~~ and sense cells ~~(34);~~

a control input ~~(10)~~ connected to the main and sense cells ~~(32,34)~~ and

main and sense cell controlled outputs ~~(4,6,44,46);~~

an output terminal ~~(12)~~ connected to one of the main cell controlled

outputs for connection to a load ~~(14);~~

a feedback circuit ~~(36)~~ for measuring the voltage across the main cell controlled outputs of the output transistor and controlling the voltage on the control input ~~(10)~~ to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs ~~(4,6)~~ falls below a predetermined value;

a reference current supply ~~(28)~~ feeding a reference current through the sense cell controlled outputs;

and a comparator ~~(18)~~ arranged to compare the voltages across the main cell outputs ~~(4,6)~~ and the sense cell outputs ~~(44,46)~~ and to output a low-current signal when the magnitude of the voltage across the main cell outputs ~~(4,6)~~ falls below that across the sense cell outputs ~~(44,46).~~

2. (CURRENTLY AMENDED) A power semiconductor device according to claim 1 wherein the feedback circuit ~~(36)~~ includes a voltage reference ~~(40)~~ and a comparator ~~(38)~~ connected across the main cell outputs ~~(4, 6)~~ for comparing the voltage across the main cell outputs with the voltage reference ~~(40)~~, the output of the comparator being connected through a diode ~~(42)~~ to the control input, the diode being orientated to pass current to change the control voltage in a direction to increase the on-resistance of the main cells ~~(32)~~ when the voltage across the main cell outputs ~~(4, 6)~~ falls below the predetermined value.

3. (CURRENTLY AMENDED) A power semiconductor transistor according to ~~claim 1 or 2~~claim 1 wherein the main ~~(32)~~ and sense ~~(34)~~ cells are FET main and sense cells and the gates ~~(8, 48)~~ of the FETs are connected in common to the control input ~~(10)~~ and the sources and drains ~~(4, 6, 44, 46)~~ of the FETs of the main and sense cells form the outputs of the FETs.

4. (CURRENTLY AMENDED) A semiconductor device according to claim 3, in the form of a high side device wherein:

the drains ~~(4, 44)~~ of the sense and main cells are connected in common to a battery terminal ~~(16);~~

the source ~~(6)~~ of the main cells is connected to the output terminal ~~(12);~~

and

the source ~~(46)~~ of the sense cells is connected to the reference current ~~(28)~~ supply, the reference current supply being a reference current sink.

5. (CURRENTLY AMENDED) A semiconductor circuit including a semiconductor device according to ~~any preceding claim~~claim 1 further comprising a load ~~(14)~~ connected to the output terminal ~~(12).~~

6. (CURRENTLY AMENDED) A method of operating a semiconductor device, the device including an output transistor ~~(2)~~ having main cells ~~(32)~~ and sense cells ~~(34),~~ and a control input ~~(10)~~ connected to the main and sense cells and main and sense cell controlled outputs ~~(4, 6, 44, 46),~~ the method including:

driving the main and the sense cells ~~(32, 34)~~ in common;

driving a load from one of the main cell controlled outputs ~~(16);~~ feeding a reference current through the sense cell controlled outputs ~~(44, 46);~~

measuring the voltage across the main cell controlled outputs ~~(4, 6)~~ and controlling the voltage on the control input ~~(10)~~ to increase the voltage across the main cell controlled outputs ~~(4, 6)~~ if the magnitude of the voltage across the main cell controlled outputs (4, 6) falls below a predetermined value; and

comparing the voltages across the main cell controlled outputs ~~(4, 6)~~ and the sense cell controlled outputs ~~(44, 46)~~ and outputting a low-current

signal when the magnitude of the voltage across the main cell controlled outputs ~~(4, 6)~~ falls below that across the sense cell controlled outputs ~~(44, 46).~~

7. (CURRENTLY AMENDED) A method according to claim 6 wherein the step of measuring the

voltage across the main cell controlled outputs is performed by:

comparing the voltage across the main cell controlled outputs ~~(4, 6)~~ with a reference voltage ~~(40)~~ using a comparator ~~(38)~~; and

driving the control input ~~(10)~~ from the output of the comparator through a diode ~~(42),~~ the diode being orientated to pass current to change the control input voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs falls below the predetermined value.